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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/358,388	07/21/1999	KAORI UMEZAWA	0039-79292-2	1515

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EXAMINER	
MAI, ANH D	
ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/358,388	Applicant(s) UMEZAWA ET AL.	
	Examiner Anh D. Mai	Art Unit 2814	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-11,14-46 and 48-53* is/are pending in the application.

4a) Of the above claim(s) *16-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-11,14,15,24-46 and 48-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Amendment

1. Amendment filed November 7, 2002 has been entered as Paper No. 31. Claims 9, 25-33, 36, 41 and 44-46 have been amended. Claims 9-11, 14-46 and 48-53 are pending. Claims 16-23 have been withdrawn.

Election/Restrictions

2. This application contains claims 16-23 drawn to an invention nonelected with traverse in Paper No. 4. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "forming thin thermal oxide films on the inner walls of the grooves" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 9-11, 14, 15, 24-46 and 48-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers et al. (U.S. Patent No. 4,571,819) in view of Lee et al. (U.S. Patent No. 4,952,524) (all cited previously).

With respect to claim 9, Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) depositing oxide films (19) in the grooves by a CVD method;

(c) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the active areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(d) annealing the oxide films (19) at a substrate temperature which is greater than or equal to 1150 °C but less than 1350 °C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized. (See Figs. 2-8).

Thus, Rogers is shown to teach all of the features of the claim with the exception of explicitly using an electrically inert organic silicon source for the CVD oxide film (19).

However, Lee teaches the electrically inert organic silicon source such as TEOS are well known in the art to be used as silicon source for the oxide film (25).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to deposit the oxide film (19) of Rogers using electrically inert organic silicon source, TEOS, as taught by Lee because electrically inert organic silicon source, TEOS, is less toxic and easy to handle. This is well known in the art.

Note that the dislocation density is an inherent result of the high temperature annealing of the substrate. Since the annealing temperature of Rogers is within the claimed range, (>1150 °C to <1300 °C), therefore, the dislocation density generated in the corresponding device region in a vicinity of the grooves (13) of Rogers is inherently less than $1/\mu m^2$.

With respect to claim 10, the depositing method of Rogers includes one of the methods as claimed.

With respect to claim 11, the ambient during the anneal of Rogers includes nitrogen gas.

With respect to claim 14, trench (13) of Rogers appears to have a depth (d) to width (l) ratio of less than 10.

With respect to claims 15 and 24, the arrangement of the grooves on the semiconductor substrate is clearly a design choice. The method of forming the STI is disclosed.

With respect to claim 30, Rogers teaches depositing the oxide films (19) in the grooves (13).

Thus, Roger is shown to teach all the features of the claim with the exception of explicitly depositing the oxide films directly on walls of the grooves.

However, Applicant admitted that "a substitute thermal oxidation film can be used or that both of these alternative can be omitted under the teaching of the paragraph beginning at line 22 of page 19", therefore, the oxide film needs not be directly deposited on walls of grooves.

With respect to claim 25, Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) depositing oxide films (19) in the grooves by a CVD method;

(c) annealing the oxide films (19) at a substrate temperature which is greater than or equal to 1150 °C but less than 1350 °C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized; and

(d) removing upper parts of the oxide films, after the annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the active areas of the semiconductor substrate serving as a top surface of a corresponding device region. (See Figs. 2-8).

With respect to the electrically inert organic silicon source and dislocation density, similar reasoning as that of claim 9 is also applied.

With respect to claim 31, the similar reasoning as that of claim 30 is also applied here.

With respect to claims 26 and 27, Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) burying oxide films (19) in the grooves (13) by a CVD method;

(c) annealing the oxide films at a substrate temperature of which is greater than or equal to 1150 °C but less than 1350 °C. (See Figs. 2-8).

With respect to the electrically inert organic silicon source, similar reasoning as that of claim 9 is also applied.

Note that the order ring structure and the etch rate of the oxide films are an inherent result of high temperature annealing of the substrate. Since the annealing temperature of Rogers is within the claimed range (>1150 °C to <1300 °C), therefore, the limitation of "higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates" as well as "Raman intensity corresponding to respective ring structures" and "an etching rate by ammonium fluoride solution of the oxide film less than 130 nm/min" are inherent result the *annealing of the substrate at high temperature*.

With respect to claims 32 and 33, the similar reasoning as that of claim 30 is also applied here.

With respect to claim 28, Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) forming a thin thermal oxidation film (16) on the inner wall of the grooves;

(c) depositing oxide films (19) on the thin thermal oxidation film by a CVD method;

(d) removing upper parts of the oxide films (19) so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as top surface of a corresponding device region; and

(e) annealing the oxide films, after the removing, at a substrate temperature which is greater than or equal to 1150 °C but less than 1350 °C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized. (See Figs. 2-8).

With respect to the electrically inert organic silicon source and dislocation density, similar reasoning as that of claim 9 is also applied.

With respect to depositing oxide films directly on the thin thermal oxidation films, Applicant admitted that "a substitute thermal oxidation film can be used or that both of these

alternative can be omitted under the teaching of the paragraph beginning at line 22 of page 19", therefore, the oxide film needs not be directly deposited on the thermal oxidation films.

With respect to claim 34, the thin thermal oxidation films (16) of Rogers are formed by thermal oxidizing inner walls of the grooves (13).

With respect to claim 29, Rogers teaches a method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions substantially as claimed including:

(a) forming a plurality of grooves (13) on part of a surface of the semiconductor substrate (10);

(b) forming thin thermal oxidation films (16) on the inner walls of the grooves;

(c) depositing oxide films (19) on the thermal oxidation films (16) in the grooves by a CVD method;

(d) annealing the oxide films (19) at a substrate temperature which is greater than or equal to 1150 °C but less than 1350 °C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is minimized; and

(e) removing upper parts of the oxide films, after the annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the active areas of the semiconductor substrate serving as a top surface of a corresponding device region. (See Figs. 2-8).

With respect to the electrically inert organic silicon source and dislocation density, similar reasoning as that of claim 9 is also applied.

With respect to claim 35, the thin thermal oxidation films (16) of Rogers are formed by thermal oxidizing inner walls of the grooves (13).

With respect to claim 36, Rogers teaches a method for forming a microelectronic structure substantially as claimed including:

(a) forming a photoresist mask layer on a substrate (10) wherein the photoresist mask layer exposed a part (12) of the substrate;

(b) forming a groove (13) in the exposed part of the substrate;

(c) depositing a layer of an insulating film (19) so as to fill the groove (13) and cover the substrate;

(d) annealing the insulating film at a temperature which is greater than or equal to 1150 °C but less than 1350 °C. (See Figs. 2-8).

Thus, Rogers is shown to teach all of the features of the claim with the exception of explicitly using an electrically inert organic silicon source to form the insulating film (19) so as to cover the mask layer (11).

With respect to forming the mask layer, Lee teaches forming a mask layer (15) under the photoresist mask (17) in the formation of groove (51) to protect the surface of the substrate from the plasma of the etch.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the mask layer of Rogers including an mask layer (15) under the photoresist mask (17) as taught by Lee to protect the surface of the substrate from the plasma.

With respect to using the electrically inert organic silicon source to form the insulating film (19), similar reasoning as that of claim 9 is also applied here.

With respect to claims 37 and 38, the duration of the annealing of Rogers encompassed the claimed duration.

With respect to claims 39 and 40, the annealing of Rogers is performed in an inert atmosphere (N_2).

With respect to claim 41, the method of Rogers further includes planarizing the insulating film (19) so that the substrate is exposed.

With respect to claim 42, the planarizing of Rogers comprises using CDE method.

With respect to claim 43, the forming the mask layer of Lee comprises forming an oxide layer (13) on the substrate.

With respect to claim 44, forming the layer of the insulating film (19) of Rogers comprises forming an oxide layer (16) on inner walls of the groove (13) and depositing the insulating material (19) on the oxide layer (16) to fill the groove.

With respect to claim 45, the depositing of insulating material (19) of Rogers comprises forming an oxide by CVD.

With respect to claim 46, the similar reasoning as that of claim 30 is also applied here.

With respect to claim 48, a taper grooves is also contemplated by Lee. (See Fig. 9).

With respect to claim 49, the depositing of the insulating film (19) of Rogers appears to deposit the insulating film at a thickness larger than a half of the width of the groove.

With respect to claim 50, the forming the mask of Rogers is configured to provide a plurality of grooves at a cross sectional view so as to define a SDG region between a couple of the grooves at the cross sectional view.

With respect to claim 51, Rogers teach all of the features of the claim with the exception of explicitly disclose the width of the SDG between the couple of the grooves (13).

However, the SDG region having a width as claimed does not appears to be critical.

Therefore, given the teaching of the references, it would have been obvious matter of design choice to form the SDG region having a width as claimed, since such a modification would have involved a mere change in the size of the SDG regions. A change in size is generally recognized as being within the level of ordinary skill in the art. See *In re Rose, 105 USPQ 237 (CCPA 1955).*

With respect to claim 52, the method of Rogers further includes forming source/drain regions (36/37) in the SDG region sandwiched by the grooves (13).

With respect to claim 53, the grooves of Rogers appears to have an aspect ratio of less than 10.

Response to Arguments

6. Applicant's arguments filed November 7, 2002 have been fully considered but they are not persuasive.

Regarding the "electrically inert organic silicon source", the organic silicon source of Lee is TEOS, therefore, the organic silicon source of Lee is inherently electrically inert, as discussed by Applicant.

Applicant cited BSG, PSG and BPSG to support his position on the organic silicon source being electrically inert. However, it is well known that BSG, PSG and BPSG are not referred to as silicon source but rather dielectric material, e.g. product. Further, although BSG, PSG and BPSG contain dopants, electrically active, but they are still "electrically inert", e.g. non-conductive.

With respect to Raman intensities measurement, the specification discloses: "Figs. 6A, 6B and 7A are the results that a structure of the oxide film according to the first embodiment of the present invention enabling reduction in dislocation density and reduction in leakage current ...". (page 21, line 17 to page 22, line 33). All of which are temperature dependent, not organic source as contended.

7. Applicant's arguments with respect to the rejection under Bose and Anon '019 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
January 21, 2003

Wael Fahmy

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800